

Hardware Unit Test Report

Set-Top Box

BFX-UH200

Ethernet RGMII Timing Test and LED status

Hardware version	FW version	Sample No.	eMMC Flash P/N
015	r05 BFX-UH200	S/N: 2154001662-01S1	KLM8G1GETF-B041

1.1 Ethernet RGMII timing test structure



Note: Ethernet cable needs 1Gb for requirement.

Command:

MDC/MDIO: signal from MAC is keeping sending, no command is required.

RGMII RX/TX command:

```
iperf3 -c IP_address -t 3600
```

1.2 Ethernet RGMII Specification

4.7.6 Ethernet Timing Specification

Figure 4-12. Management Data Timing Diagram

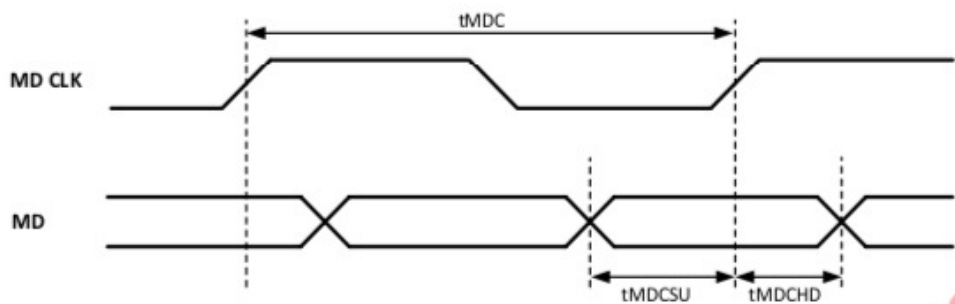


Table 4-10. Management Data Timing Specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
tMDC	MDC clock Period	400	500		ns	From MAC
tMDCS U	Setup time to rising edge of MDC	10			ns	
tMDCH D	Hold time to rising edge of MDC	10			ns	

Figure 4-13. RMII Timing Diagram

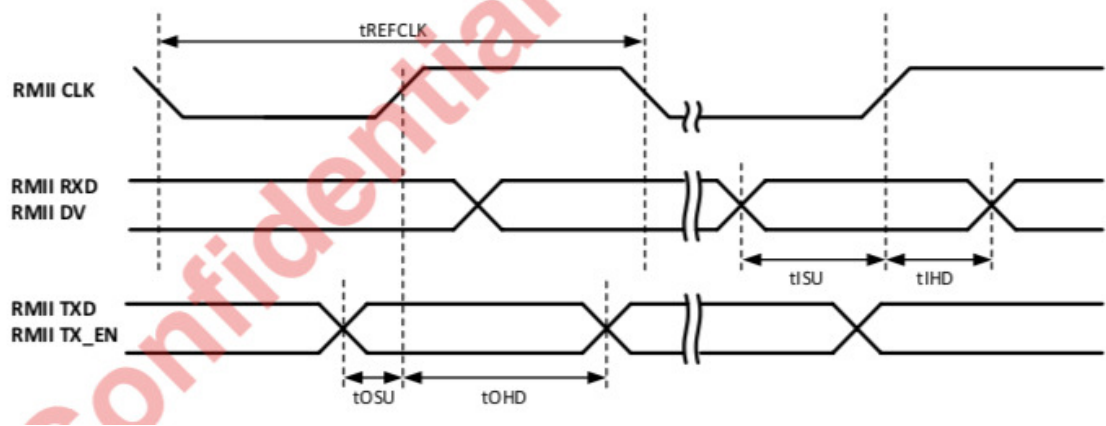


Table 4-11. RMII Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tREFCLK	RMII clock period		20		ns	50MHz from PHY
tOSU	TXD & TX_EN setup time to rising edge of RMII clock	1.8	10		ns	To PHY

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tOHD	TXD & TX_EN hold time to rising edge of RMII clock	1.4	10		ns	To PHY
tISU	RXD & DV setup time to rising edge of RMII clock	1.0	10		ns	From PHY
tIHD	RXD & DV hold time to rising edge of RMII clock	1.0	10		ns	From PHY

Figure 4-14. RGMII Receive Timing Diagram

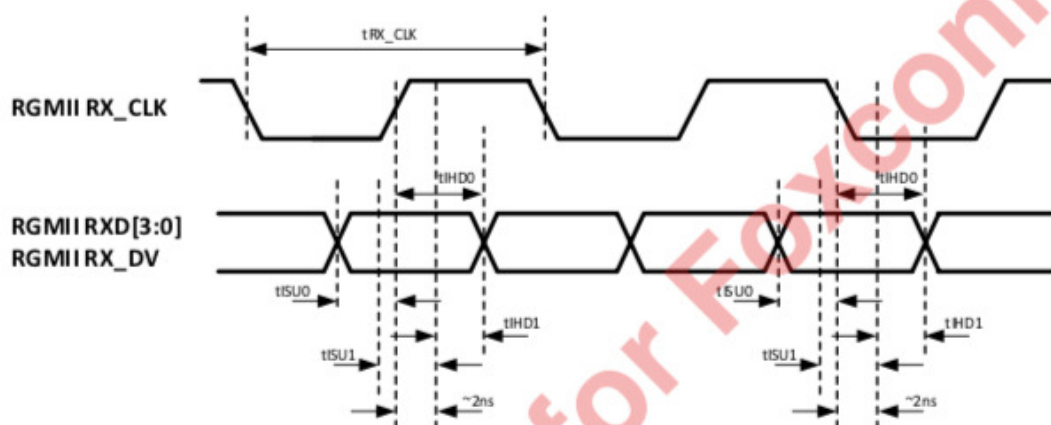


Table 4-12. RGMII Receive Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
t_{RX_CLK}	RGMII RX_CLK clock period		8		ns	125MHz from PHY
t_{SETUP}	RXD[3:0] & RX_DV setup time (PHY internal delay enabled)	1.2			ns	From PHY
t_{HOLD}	RXD[3:0] & RX_DV hold time (PHY internal delay enabled)	1.2			ns	From PHY
t_{SKEW}	RXD[3:0] & RX_DV skew between these 5 signals (PHY internal delay disabled)	-0.5		0.5	ns	From PHY

When PHY internal delay is enabled, check setup/hold timing.

When PHY internal delay is disabled, check signal skew.

Note: t_{SKEW} did not define in signal timing, so the measurement is RX_CLK vs RXD0 which is checked with Amlogic.

Figure 4-15. RGMII Transmit Timing Diagram

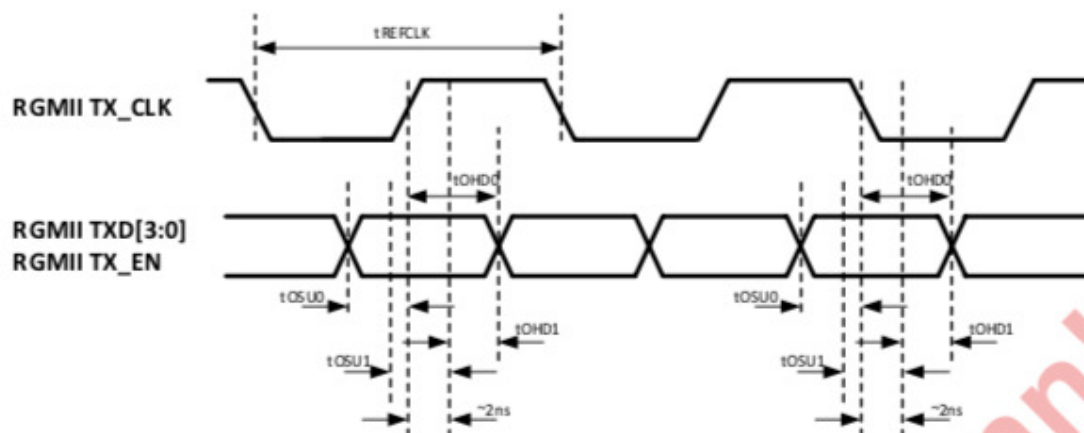


Table 4-13. RGMII Transmit Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
t_{TX_CLK}	RGMII TX_CLK clock period		8		ns	125MHz to PHY
t_{OSU}	TXD & TX_EN setup time to rising edge of RGMII clock (no clock delay added)	1			ns	From PHY
	TXD & TX_EN setup time to rising edge of RGMII clock (clock delay added)	-0.9			ns	From PHY
t_{OHD}	RXD & DV hold time to rising edge of RGMII clock (no clock delay added)	0.8			ns	From PHY
	RXD & DV hold time to rising edge of RGMII clock (clock delay added)	2.7			ns	From PHY

Note: The RXD at t_{OHD} define is wrong description, checked with Amlogic and correct to TXD.

1.3 Test Result and picture**1.3.1 Management Data Timing**

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tMDC	MDC clock Period	400	500	--	616	ns	Pass
tMDCSU	Setup time to rising edge of MDC	10	--	--	296	ns	Pass
tMDCHD	Hold time to rising edge of MDC	10	--	--	304	ns	Pass

Note: D4 is the longest trace, D0 is the shortest trace

1.3.2 RMII Timing

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tREFCLK	RMII clock Period	--	20	--	40	ns	Pass
tOSU	TXD & TX_EN setup time to rising edge of RMII clock	1.8	10	--	10	ns	Pass
tOHD	TXD & TX_EN hold time to rising edge of RMII clock	1.4	10	--	10	ns	Pass
tISU	RXD & DV setup time to rising edge of RMII clock	1.0	10	--	1.2	ns	Pass
tIHD	RXD & DV hold time to rising edge of RMII clock	1.0	10	--	19.6	ns	Pass

1.3.3 RGMII Receive Timing

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tRX_CLK	RGMII RX_CLK clock period	--	8	--	8	ns	Pass
tISU	RXD[3:0] setup time	1.2	--	--	4.56	ns	Pass
tIHD	RXD[3:0] hold time	1.2	--	--	8.208	ns	Pass
tSKEW	RXD[3:0] skew between these 5 signal	-0.5	--	0.5	0.144	ns	Pass

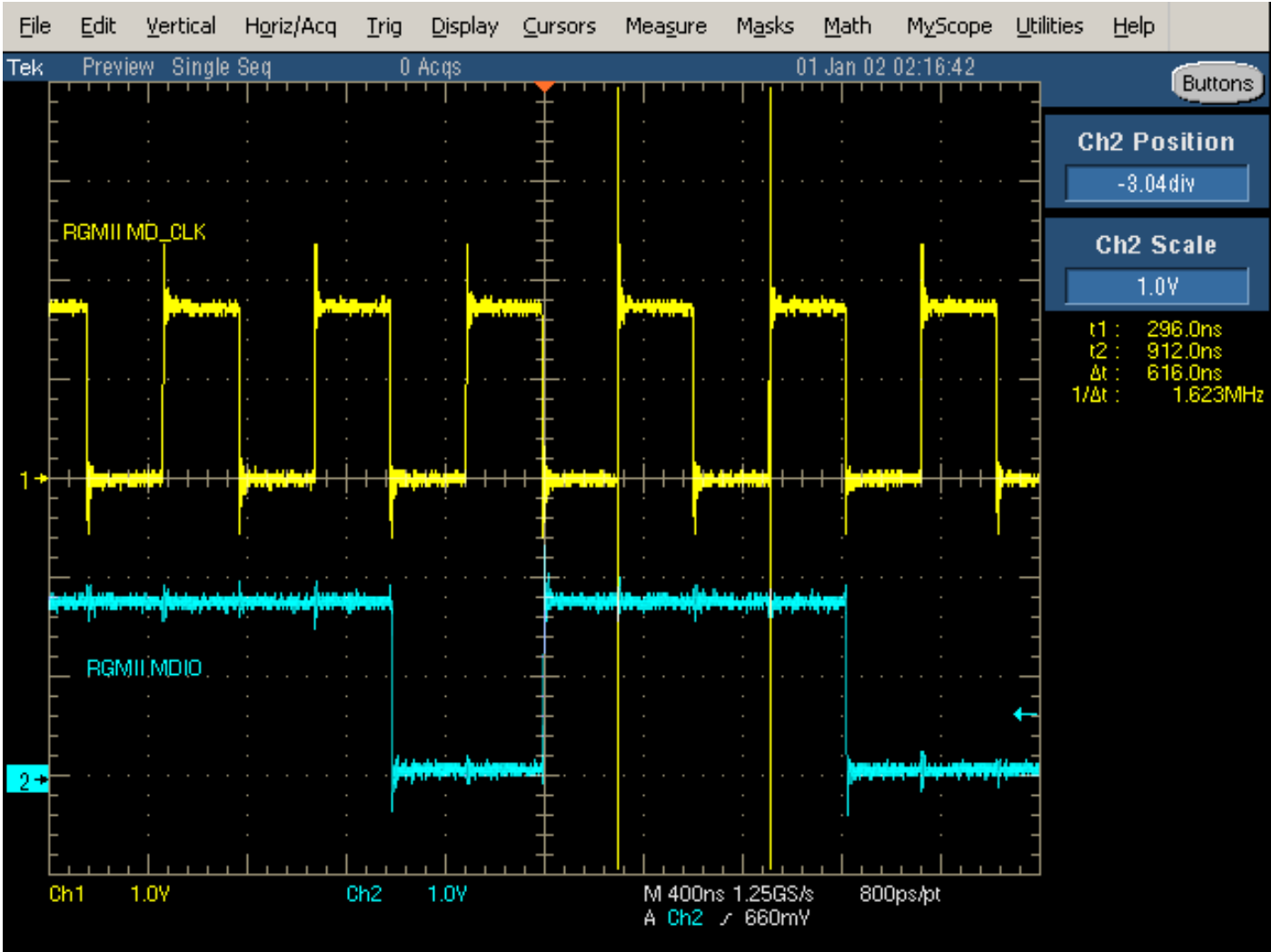
1.3.4 RGMII Transmit Timing

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tTX_CLK	RGMII TX_CLK clock period	--	8	--	8	ns	Pass
tOSU	TXD[3:0] setup time	1	--	--	6.32	ns	Pass
tOHD	TXD[3:0] hold time	0.8	--	--	5.68	ns	Pass

1.3.5 Picture of MDC timing

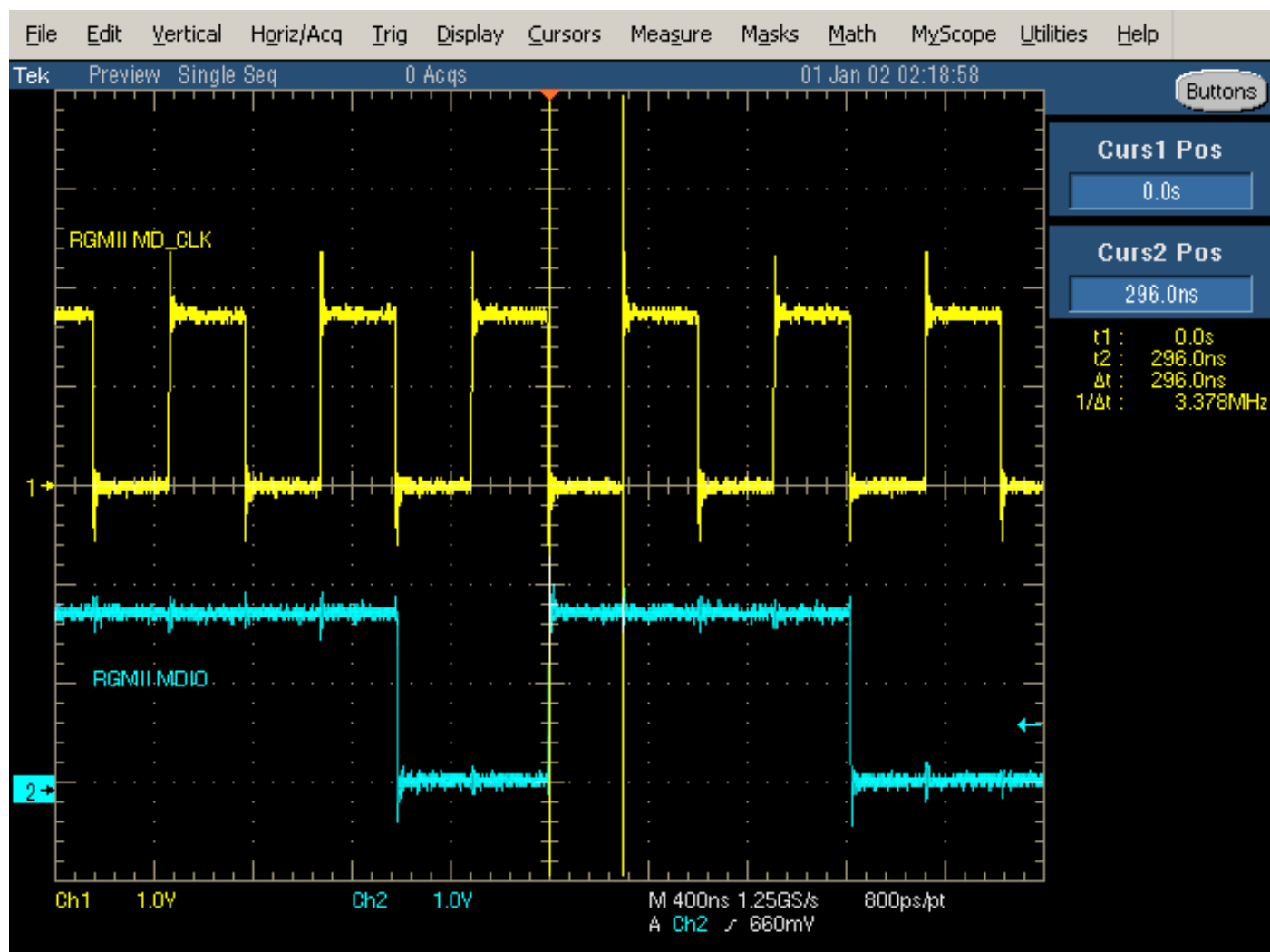
1.3.5.1 MDC - tMDC

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tMDC	MDC clock Period	400	500	--	616	ns	Pass



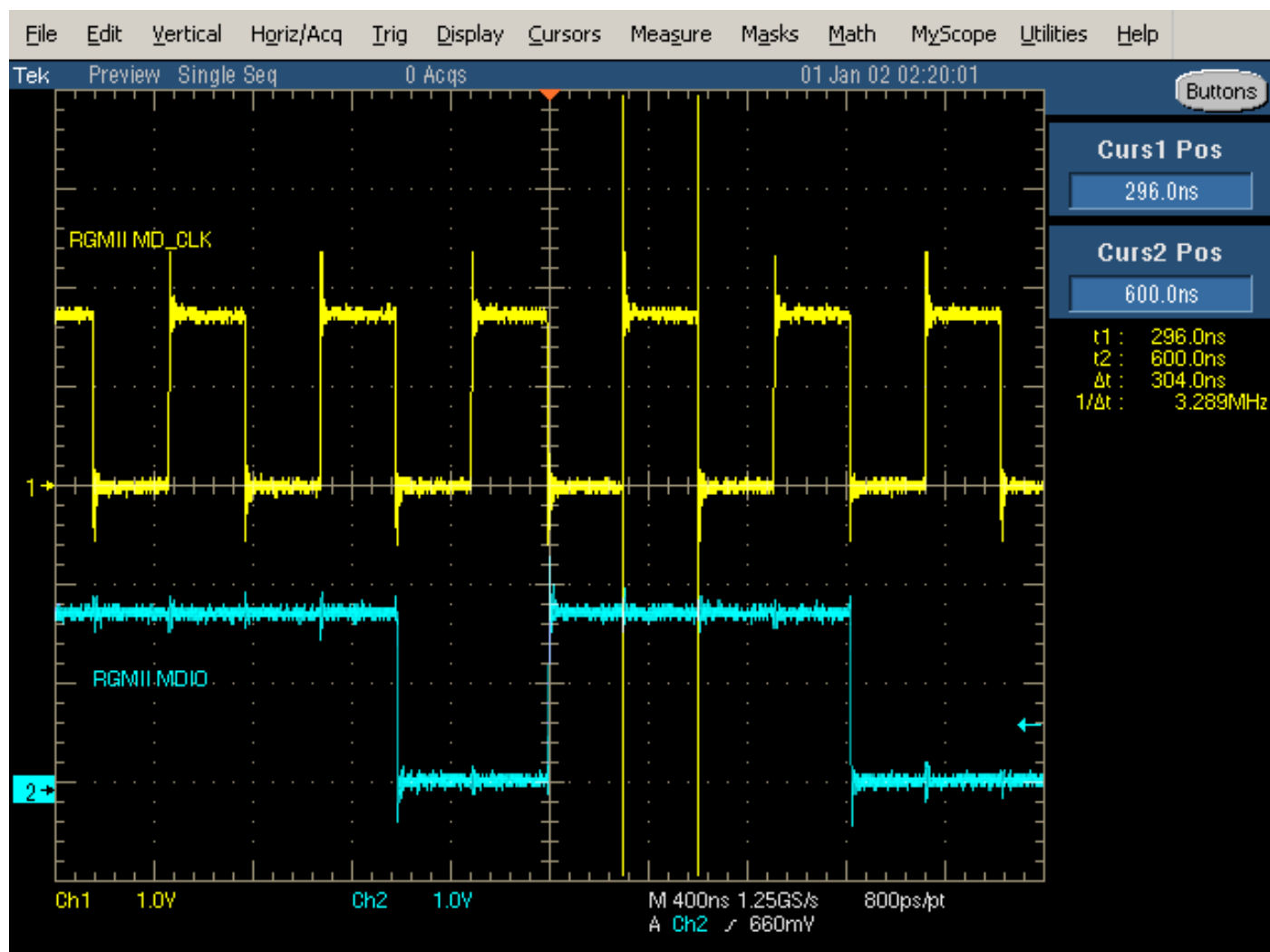
1.3.5.2 MDC - tMDCSU (Setup time to rising edge of MDC)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tMDCSU	Setup time to rising edge of MDC	10	--	--	296	ns	Pass



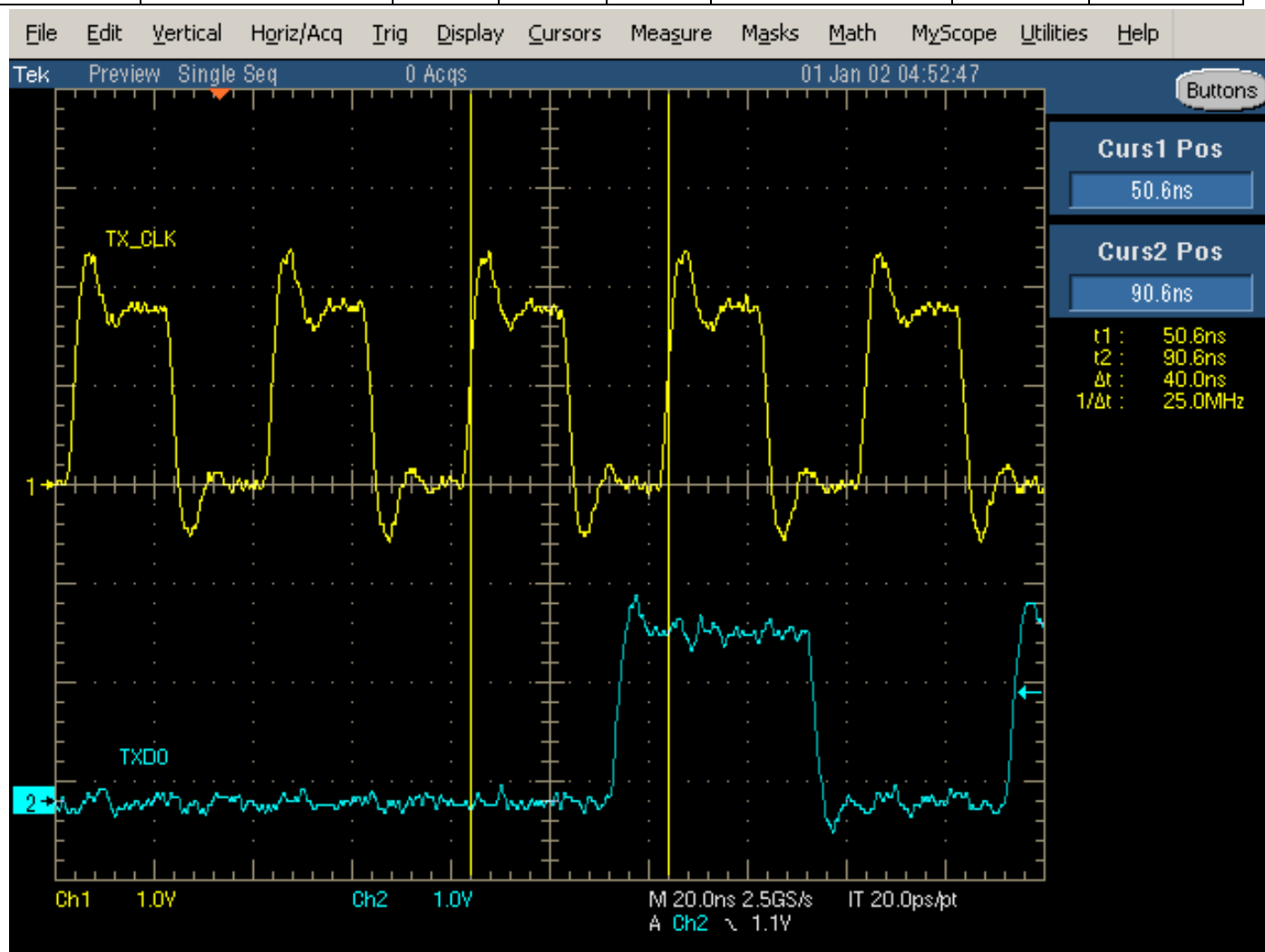
1.3.5.3 MDC - tMDCHD (Hold time to rising edge of MDC)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tMDCHD	Hold time to rising edge of MDC	10	--	--	304	ns	Pass



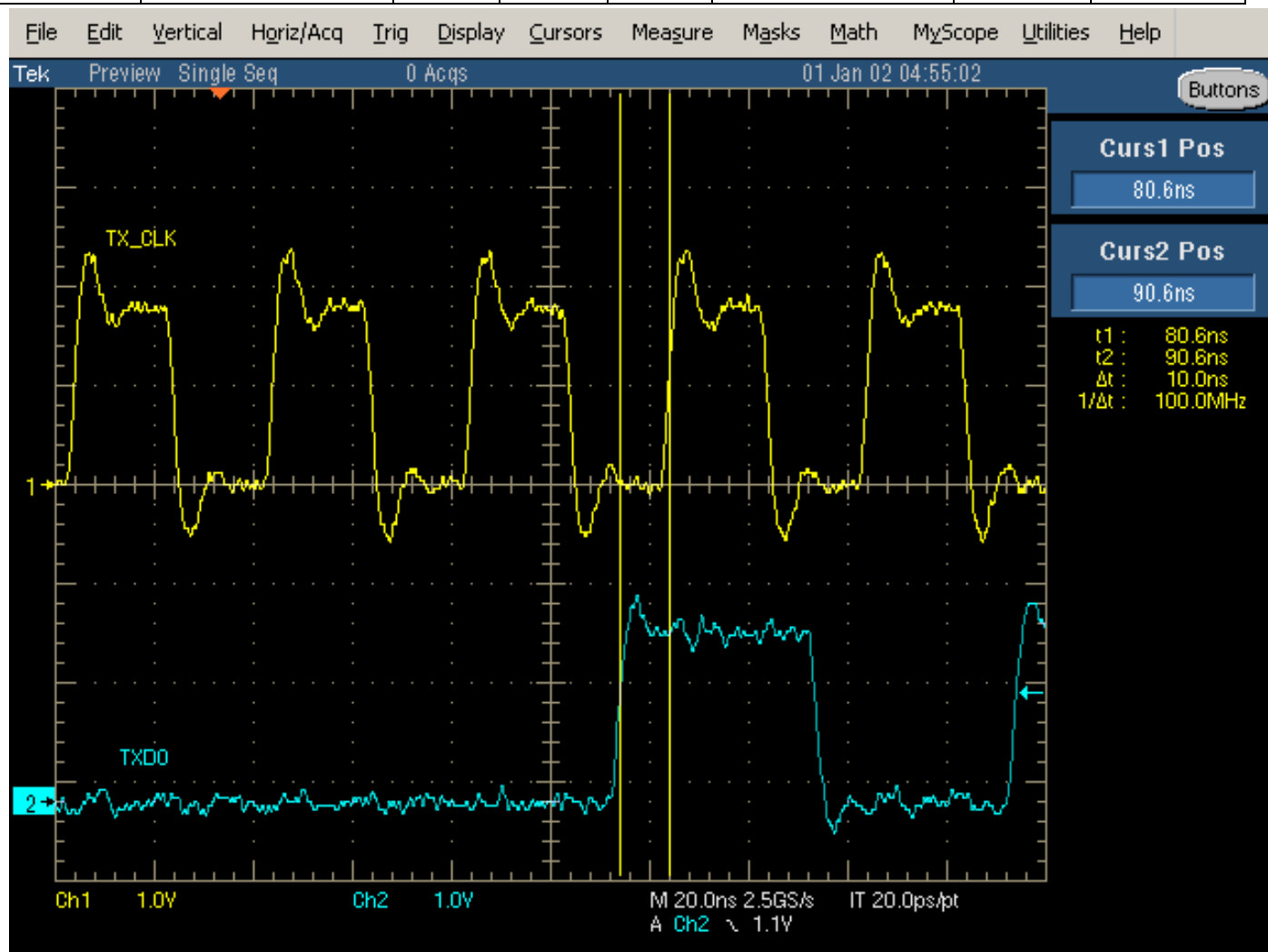
1.3.6 Picture of RMII timing**1.3.6.1 RMII - tREFCLK (RMII clock Period)**

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tREFCLK K	RMII clock Period	--	20	--	40	ns	Pass



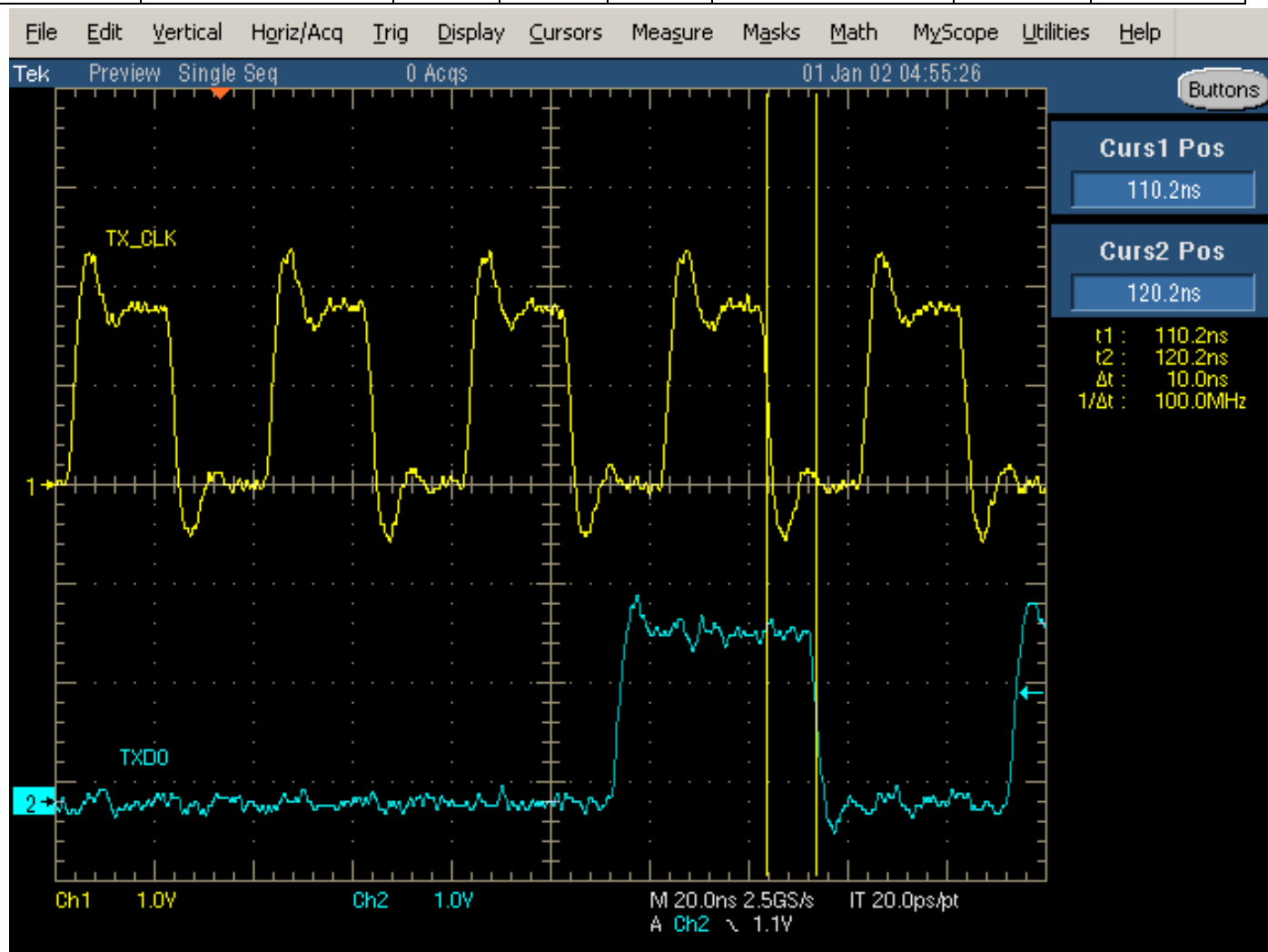
1.3.6.2 RMII - tOSU (setup time to rising edge of RMII clock)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tOSU	TXD & TX_EN setup time to rising edge of RMII clock	1.8	10	--	10	ns	Pass



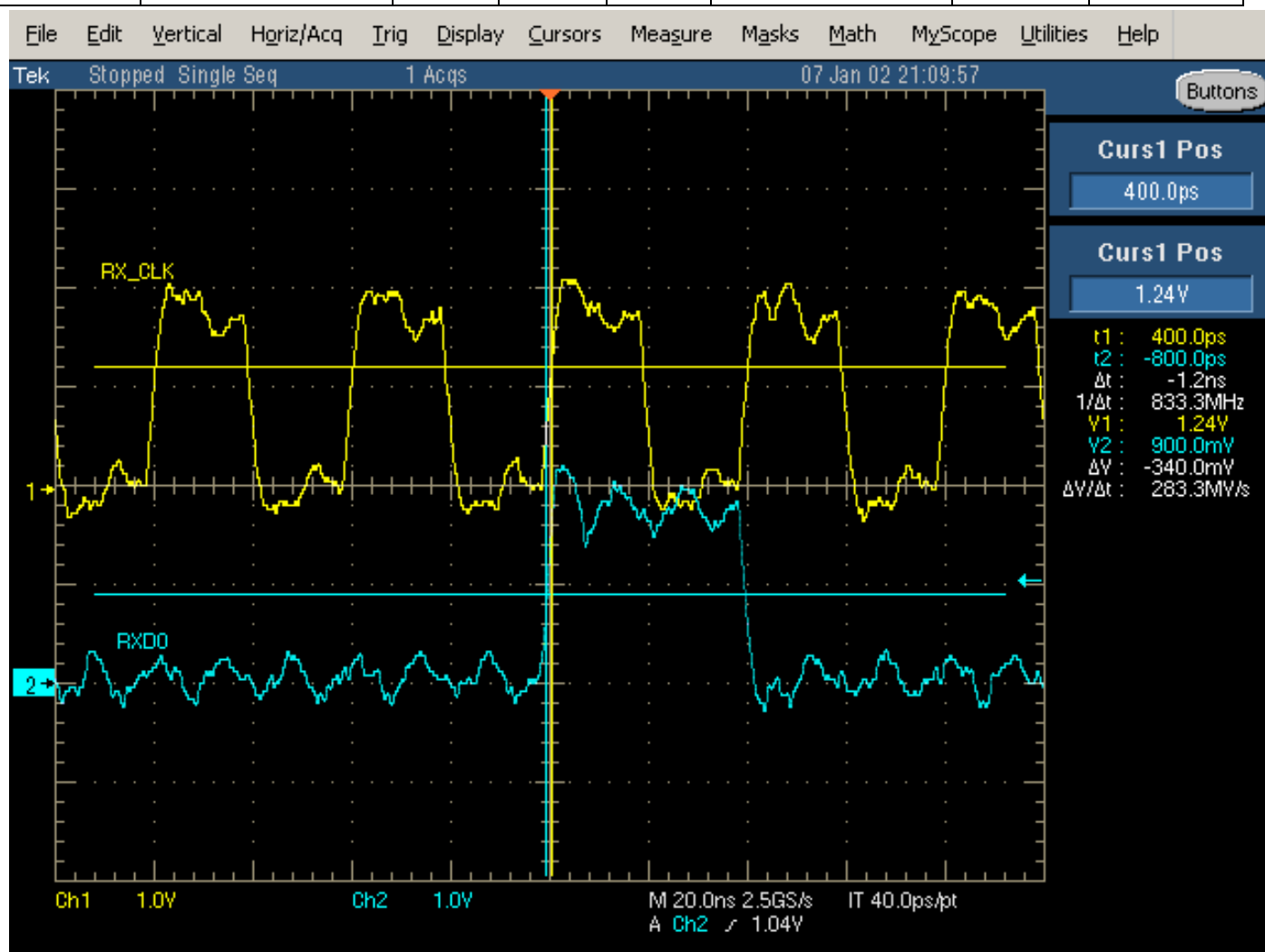
1.3.6.3 RMII - tOHD (hold time to rising edge of RMII clock)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tOHD	TXD & TX_EN hold time to rising edge of RMII clock	1.4	10	--	10	ns	Pass



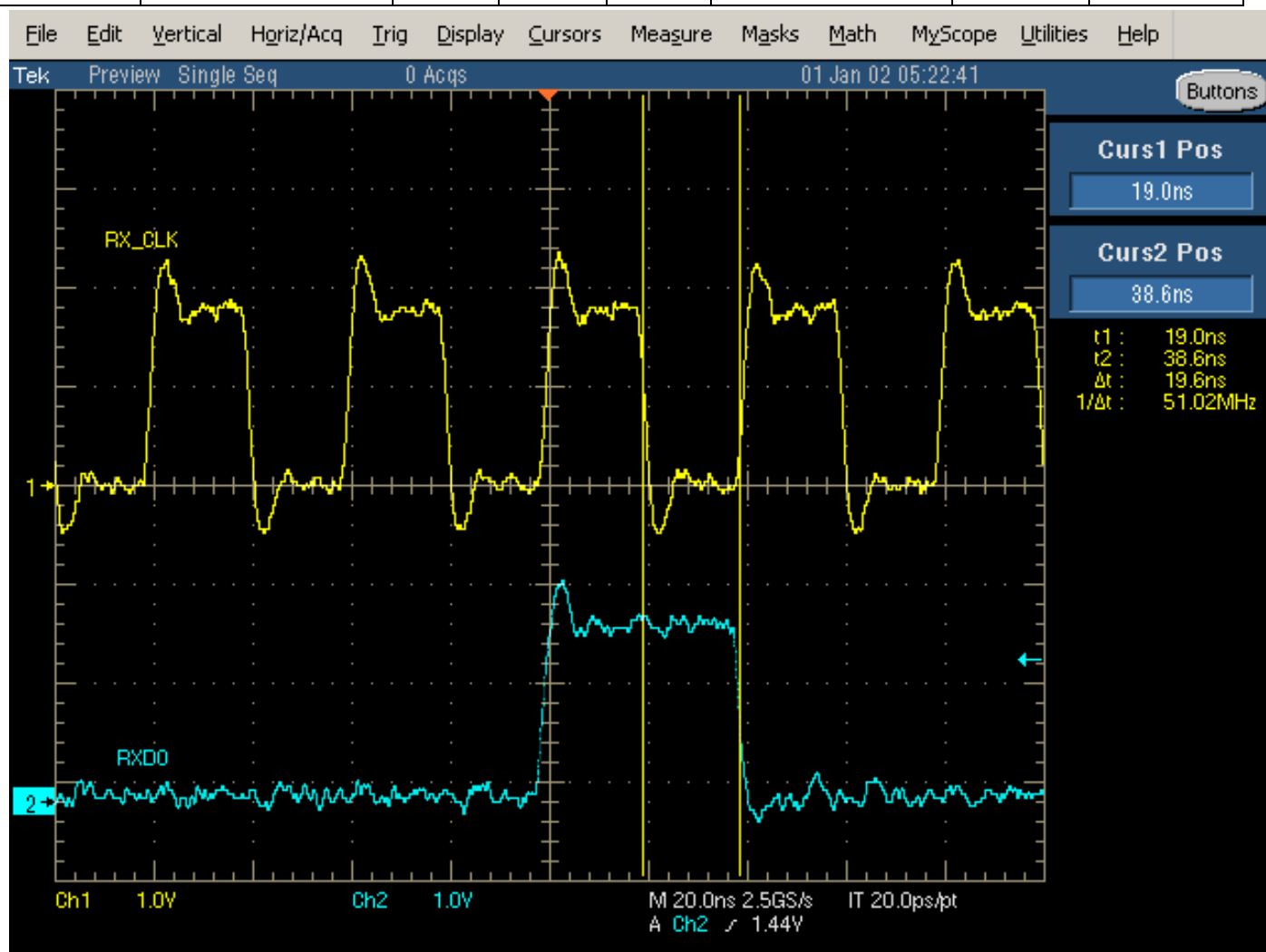
1.3.6.4 RMII - tISU (setup time to rising edge of RMII clock)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tISU	TXD & DV setup time to rising edge of RMII clock	1.0	10	--	1.2	ns	Pass



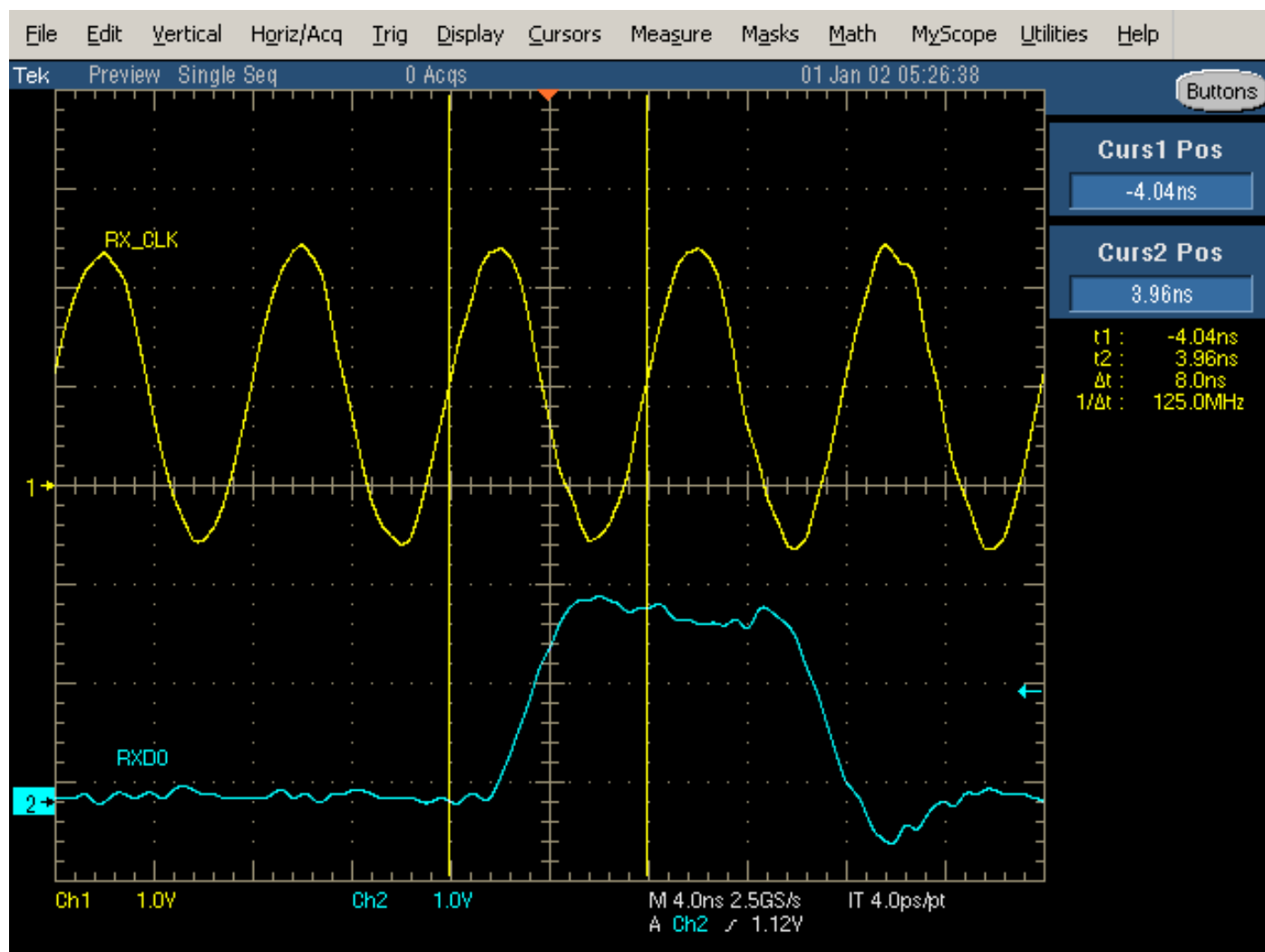
1.3.6.5 RMII - tIHD (hold time to rising edge of RMII clock)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tIHD	TXD & DV hold time to rising edge of RMII clock	1.0	10	--	19.6	ns	Pass



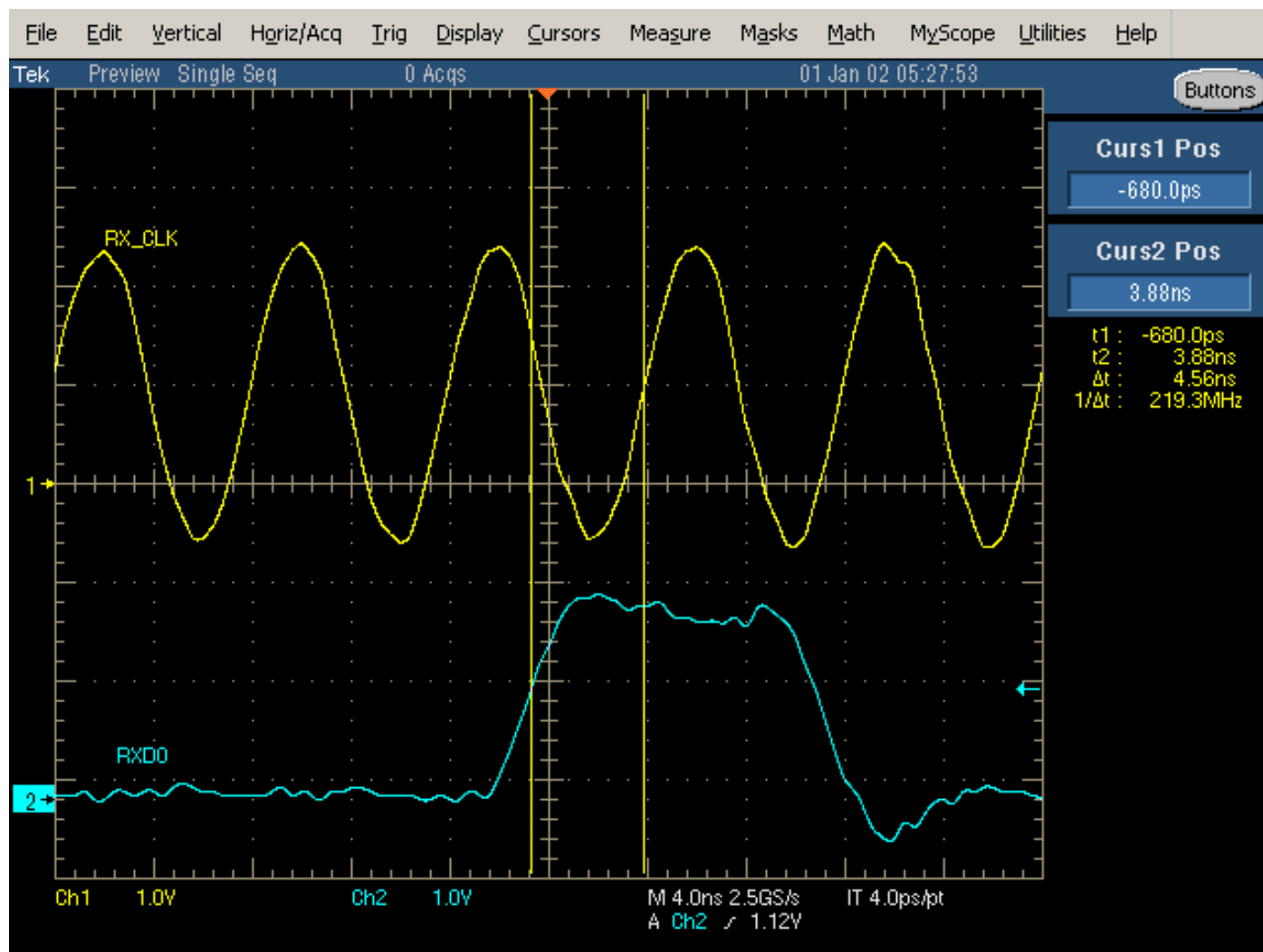
1.3.7 Picture of RGMII Receive Timing**1.3.7.1 RGMII Receive Timing – RX clock (RGMII RX_CLK clock period)**

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tRX_CLK	RGMII RX_CLK clock period	--	8	--	8	ns	Pass



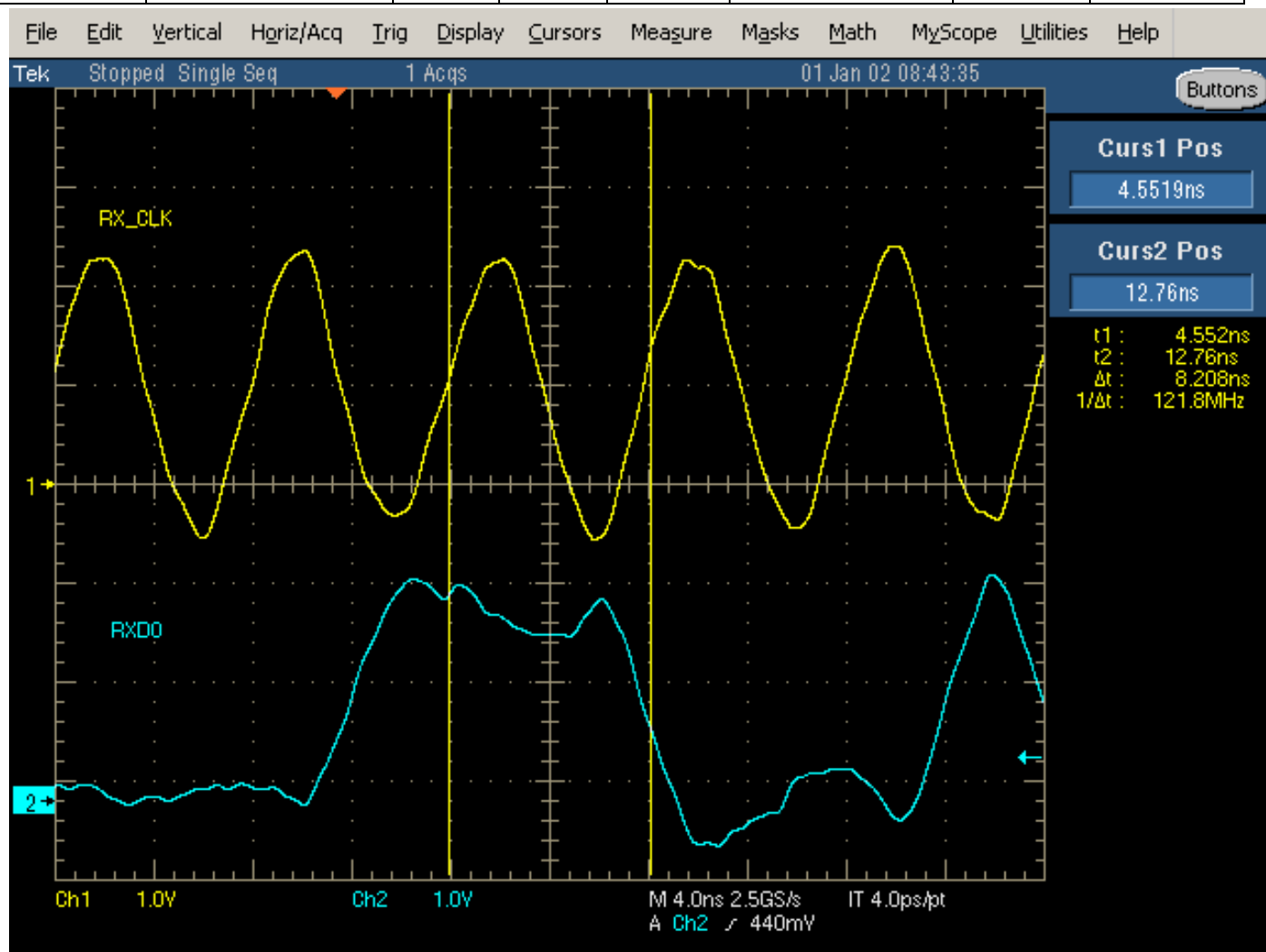
1.3.7.2 RGMII Receive Timing - tISU (RXD[3:0] setup time)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tISU	RXD[3:0] setup time	1.2	--	--	4.56	ns	Pass



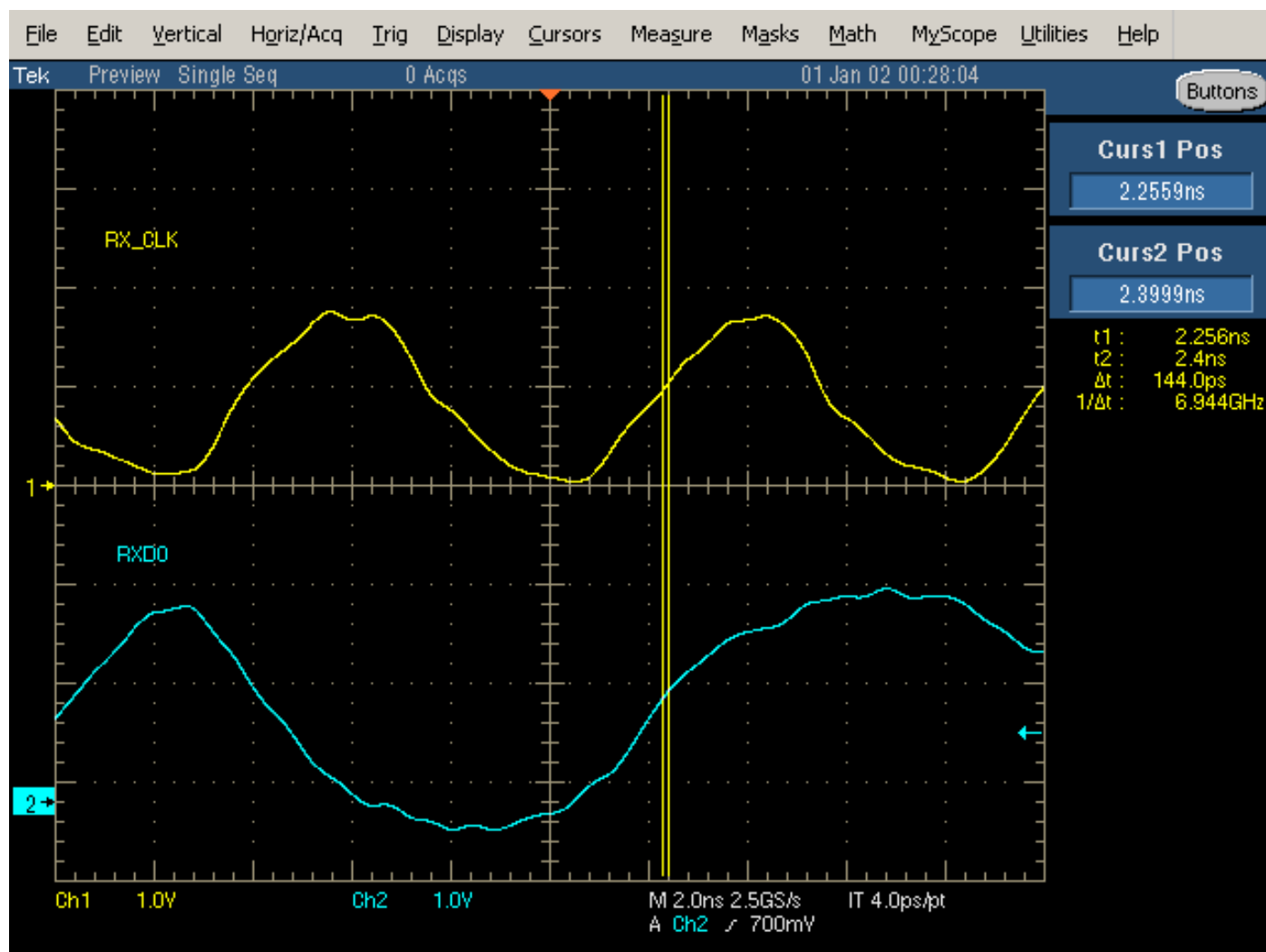
1.3.7.3 RGMII Receive Timing - tIHD (RXD[3:0] hold time)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tIHD	RXD[3:0] hold time	1.2	--	--	8.208	ns	Pass



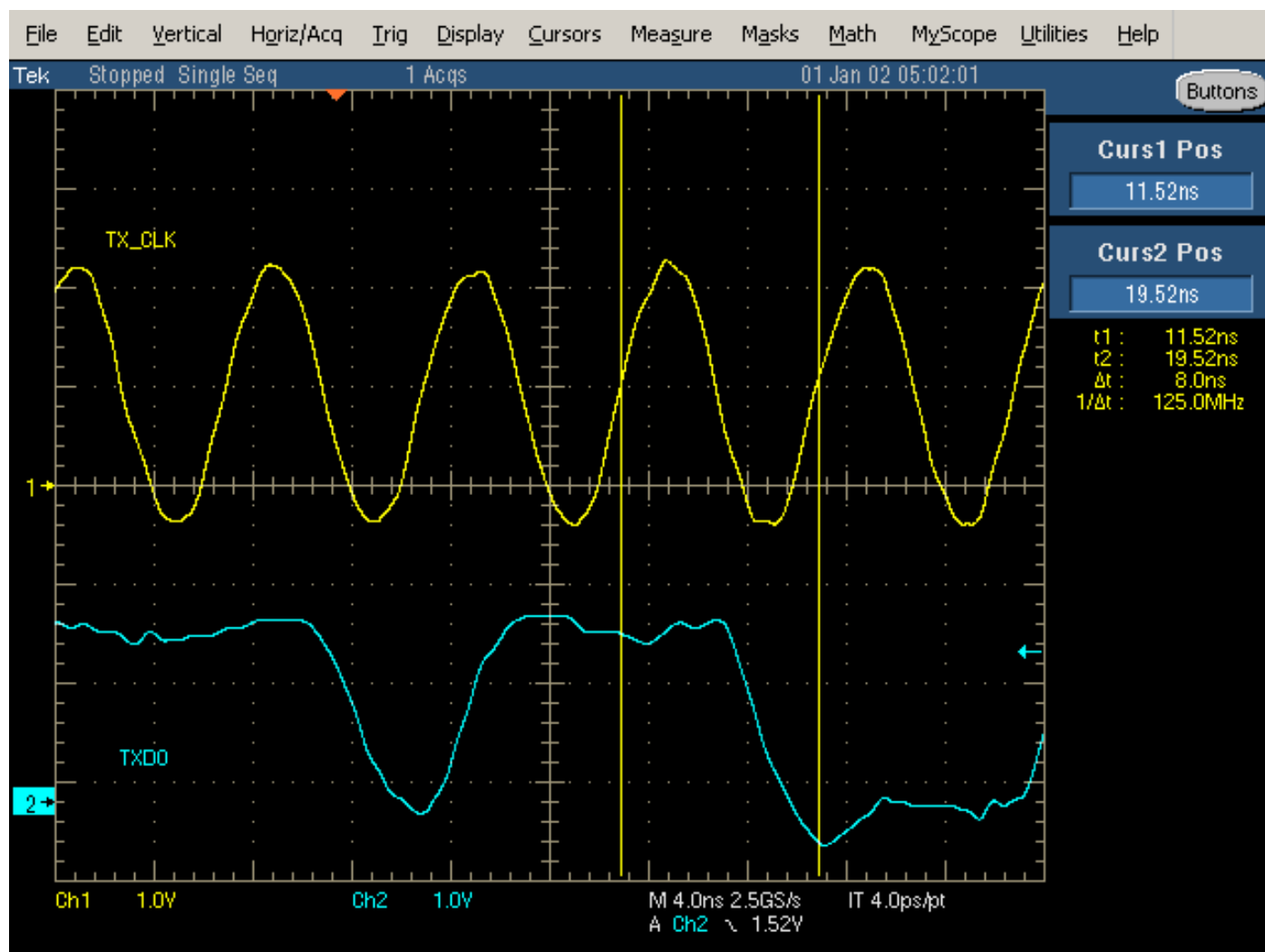
1.3.7.4 RGMII Receive Timing - tSKEW (RXD[3:0] skew between these 5 signal)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tSKEW	RXD[3:0] skew between these 5 signal	-0.5	--	0.5	0.144	ns	Pass



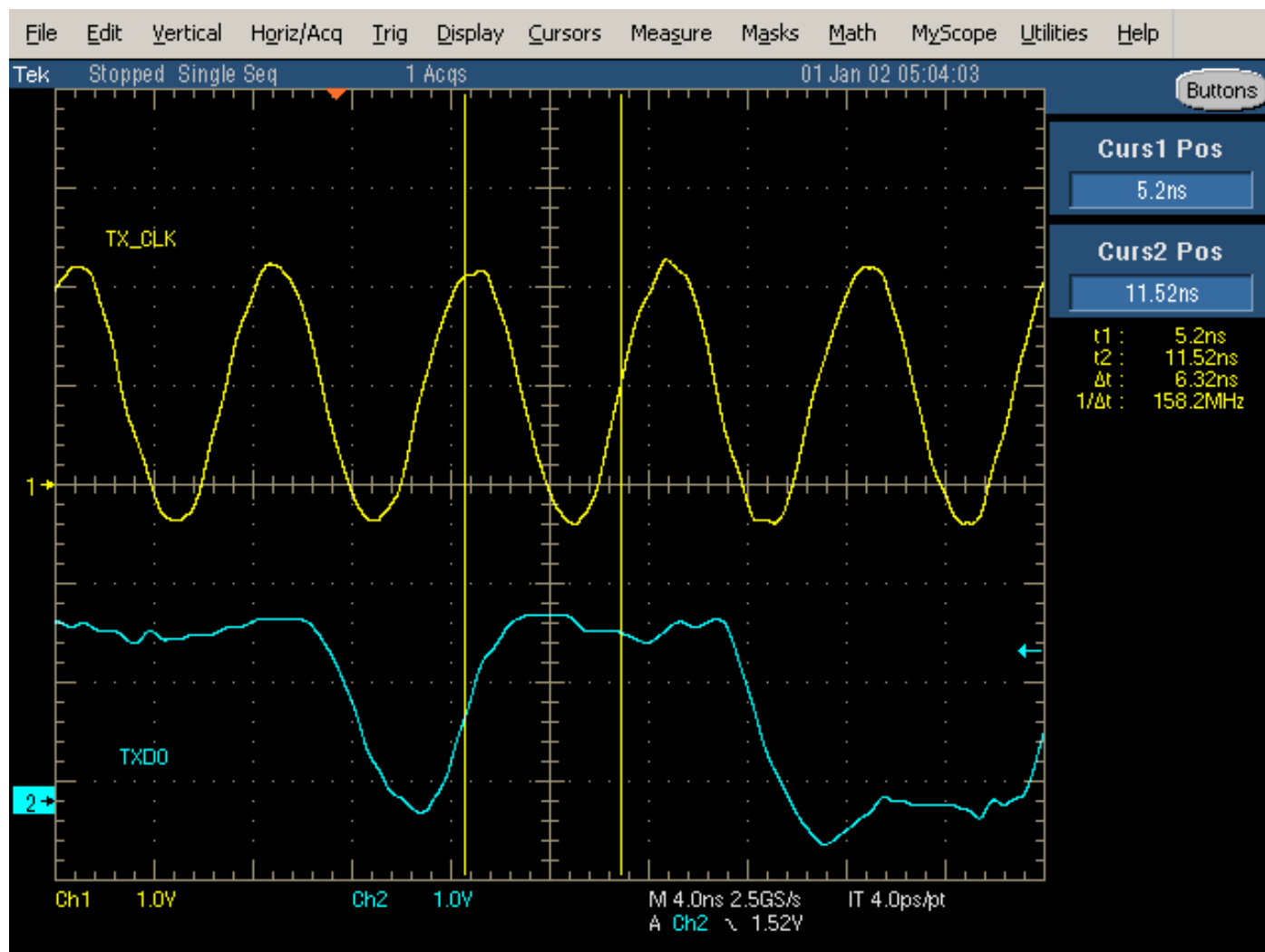
1.3.8 Picture of RGMII Transmit Timing**1.3.8.1 RGMII Transmit Timing – TX clock (RGMII TX_CLK clock period)**

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tTX_CLK	RGMII TX_CLK clock period	--	8	--	8	ns	Pass



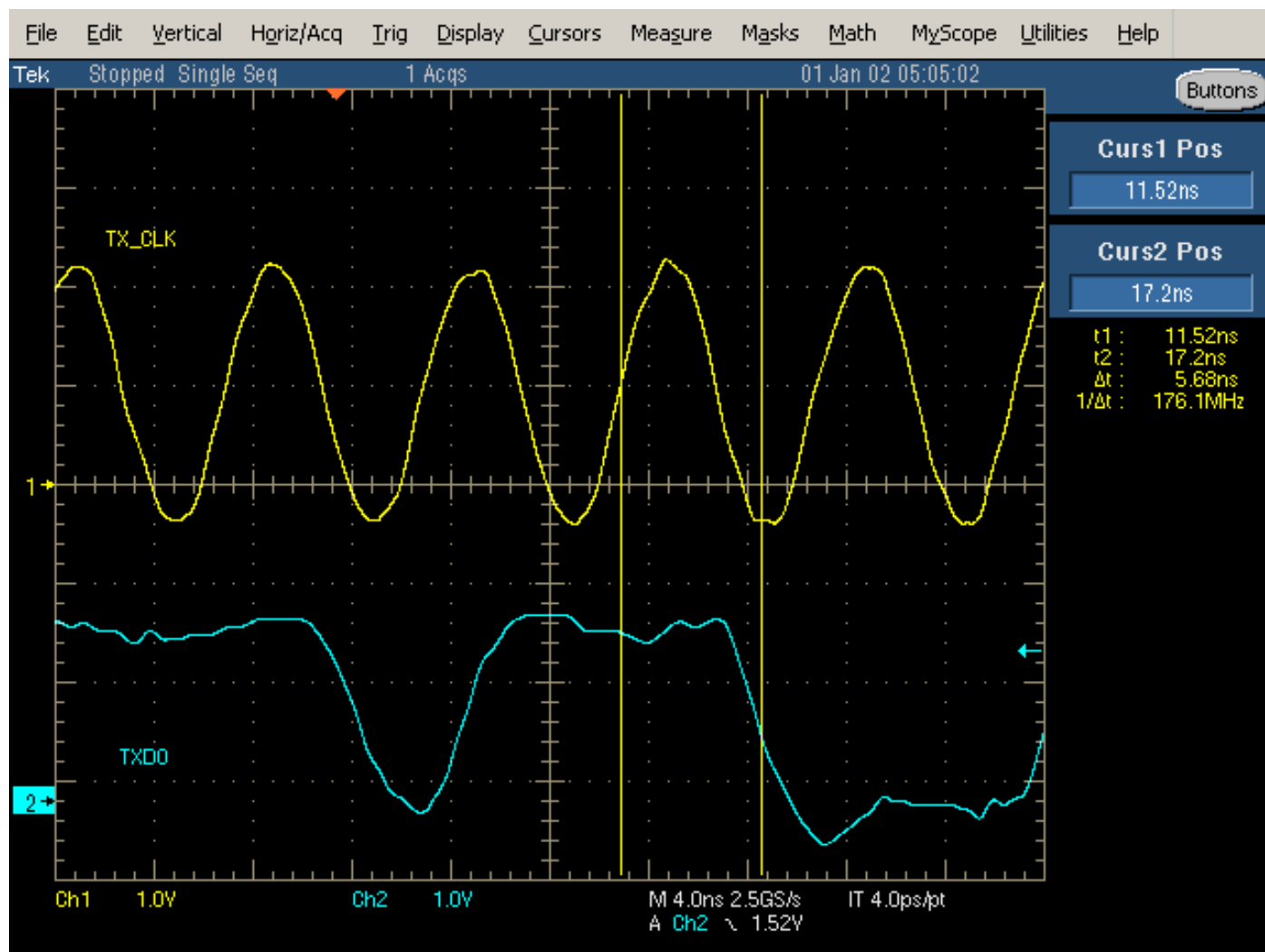
1.3.8.2 RGMII Transmit Timing - tOSU (TXD[3:0] setup time)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tOSU	TXD[3:0] setup time	1	--	--	6.32	ns	Pass



1.3.8.3 RGMII Transmit Timing - tOHD (RXD[3:0] hold time)

Test Item		Specification			Result	Unit	Pass / Fail
Symbol	Parameter	Min.	Typ.	Max.			
tOHD	TXD[3:0] hold time	0.8	--	--	5.68	ns	Pass



1.4 LED status

1.4.1 LED function

Ethernet LED on RJ45 has 2 LED indicators, one is green LED and the other is orange LED.

Green LED: Link function, when Ethernet cable plugs onto RJ45, the Green LED blinks.

2 seconds is per cycle, every cycle blinks 1 second.

Orange LED: Active function, when RTL8211F gets data, the orange LED blinks irregularly.

Note: The ACTIVE LED do not define 10/100/1000 Mbps. Just any functional Ethernet cable plugged-in can work. The LINK LED defines 100M/1000M bps for indication. Please see figure 1.4-1~1.4-4.

1.4.2 LED condition

Plugged-in Ethernet cable to RJ45 connector from Ethernet Hub and checks green LED blinks or not.

Check orange LED blinks irregularly after plugged-in Ethernet cable to RJ45 connector, the Ethernet hub will send broadcast network package to device and the orange LED will blink.

1.4.3 Test Result.



Figure 1.4-1 LINK LED



Figure 1.4-2 ACTIVE LED

Figure 1.4-3 100M cable plugged-in of LINK/ACTIVE LEDs

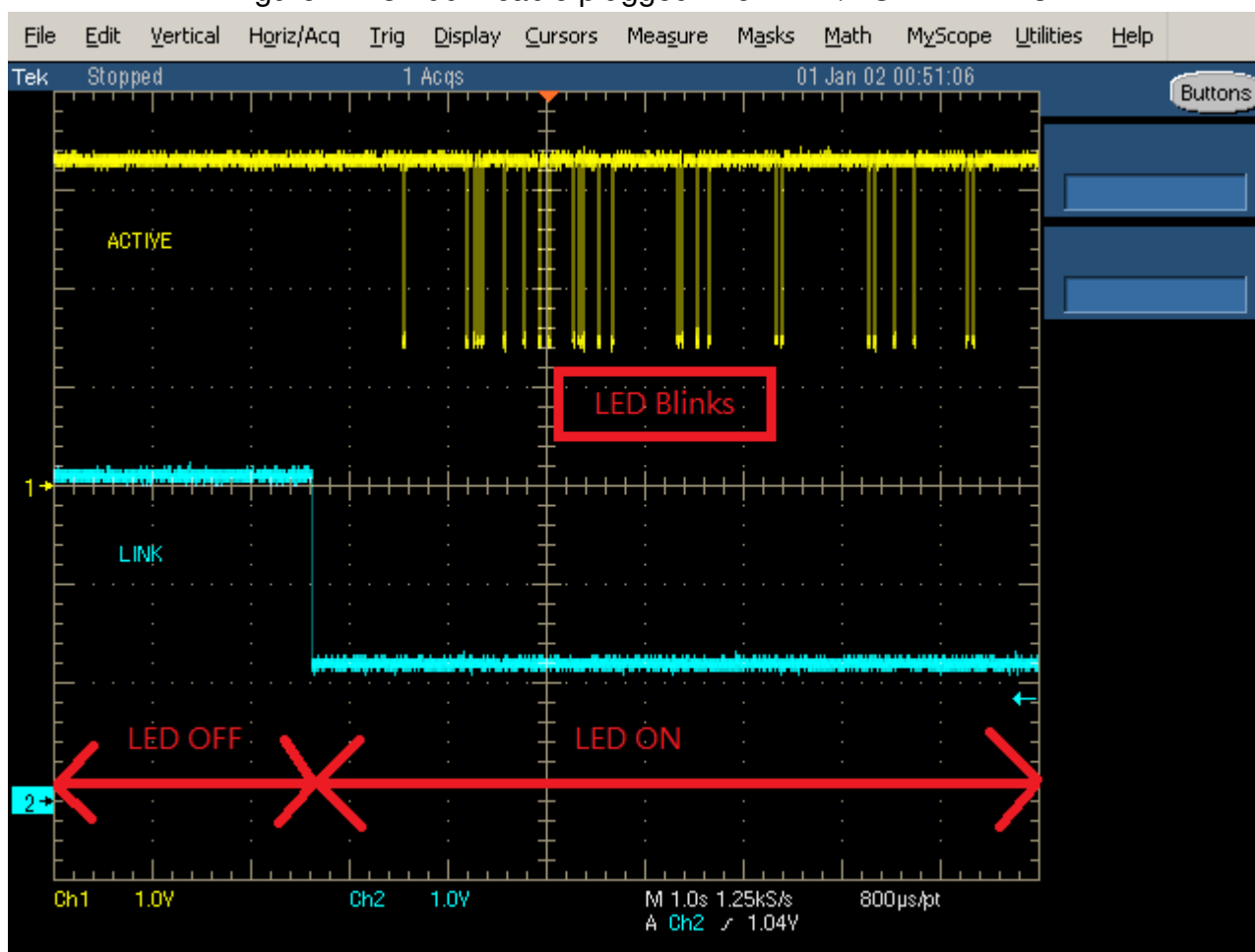
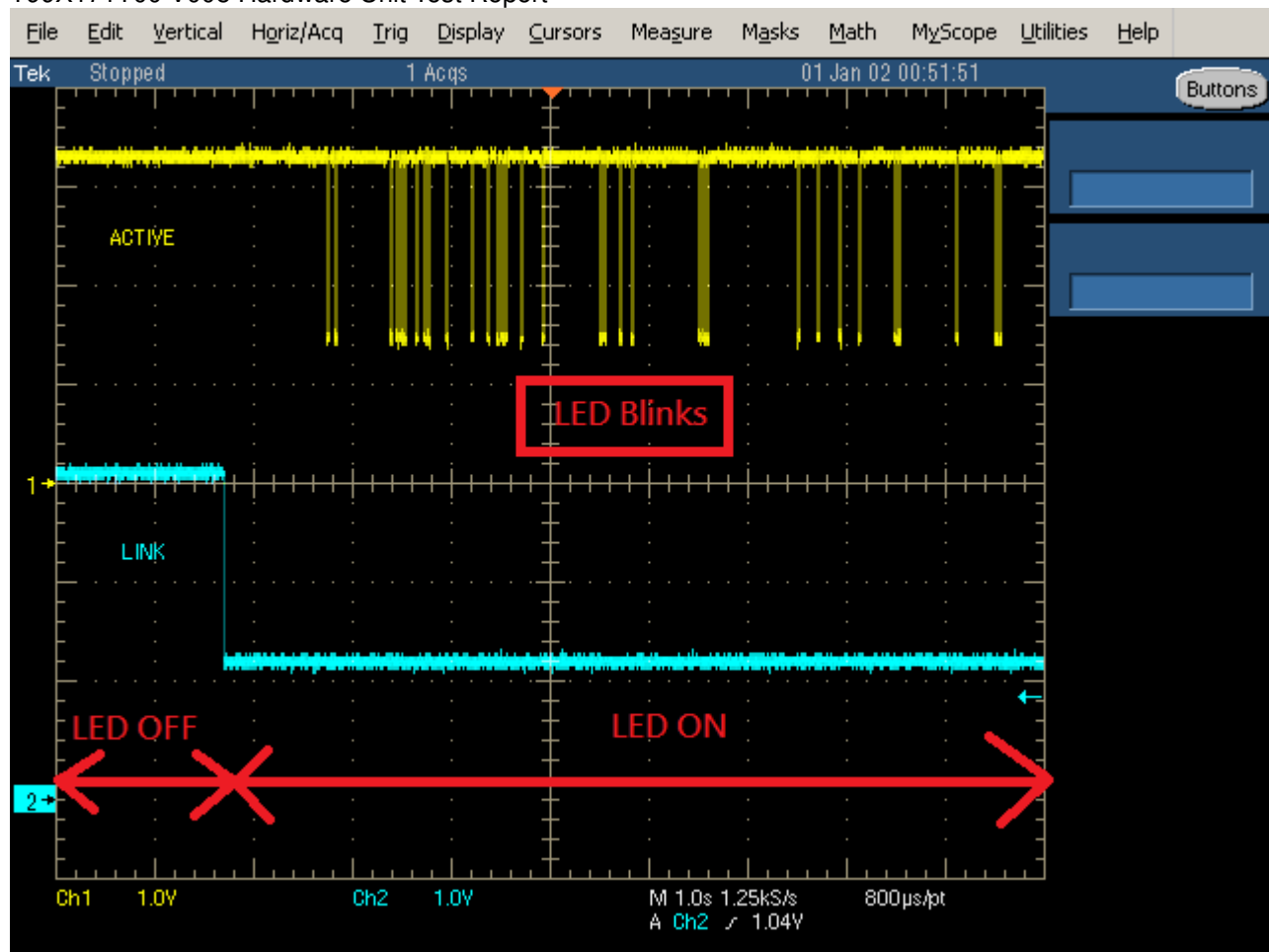


Figure 1.4-4 1000M cable plugged-in of LINK/ACTIVE LEDs

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So the test results are pass. Both LEDs can work normally.